CLAIM AMENDMENTS

1. - 28. (Cancelled)

29. (Previously presented) A method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit device, said method comprising the steps of:

Initially providing a substrate;

thereafter configuring said substrate to comprise a wiring bond pad comprising only a single metal layer, wherein said single metal layer comprises a layer comprised of only one type of metal and does not share said layer with any other material;

thereafter positioning at least one integrated circuit device below said wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring said wiring bond pad to comprise said a single metal layer;

thereafter locating a buffer and bonding layer immediately above said single metal layer;

thereafter locating said single metal layer above a plurality of intermetal dielectric layers; and

thereafter locating said at least one integrated circuit device below said plurality of intermetal dielectric layers, wherein said single metal layer comprises a metal-8 layer, thereby preventing a wiring bond stress-induced facture in said wiring bond pad.

30. (Original) The method of claim 29 wherein said plurality of intermetal dielectric layers comprises at least IMD-1 to IMD-7 layers.

31. (Original) The method of claim 29 wherein said metal-8 layer comprises a copper layer.

32. (Previously presented) A method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit device, said method comprising the steps of:

providing a substrate;

thereafter configuring said substrate to comprise a wiring bond pad to comprise a single metal layer, wherein said single metal layer does not share said single metal layer with any other material;

thereafter positioning at least one integrated circuit device below said wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring said wiring bond pad to comprise a single metal layer;

thereafter locating a buffer and bonding layer immediately above said single metal layer;

thereafter locating said single metal layer above a plurality of intermetal dielectric layers, wherein said plurality of intermetal dielectric layers comprises at least IMD-1 to IMD-7 layers; and

thereafter locating said at least one integrated circuit device below said plurality of intermetal dielectric layers, wherein said single metal layer comprises a metal-8 layer of copper;

thereafter forming a layer of aluminum film above said single metal layer, wherein said layer of aluminum film above said single metal layer comprises a buffer and bonding layer, thereby preventing a wiring bond stress-induced facture in said wiring bond pad.

33. (Original) The method of claim 32 wherein said layer of aluminum film formed above said single metal layer comprises a layer having a thickness in a range of and including 10KÅ to 20KÅ.

34. (Previously presented) The method of claim 32 wherein said single metal layer comprises a copper layer having a thickness of approximately 10KÅ.

35. (Previously presented) The method of claim 32 wherein said single metal layer comprises a copper layer having a thickness of approximately 12KÅ.

36. (Previously presented) The method of claim 32 wherein said single metal layer comprises a copper layer having a thickness of approximately 14KÅ.

37. (Previously presented) The method of claim 32 wherein said single metal layer comprises a copper layer having a thickness of approximately 16KÅ.

38. (Previously presented) The method of claim 32 wherein said single metal layer comprises a copper layer having a thickness of approximately 18KÅ.

39. (Previously presented) A method for forming a wiring bond pad utilized in wire bonding operations on an integrated circuit device, said method comprising the steps of:

providing a substrate;

configuring on said substrate, a wiring bond pad comprising a single metal layer, wherein said single metal layer comprises a copper layer;

thereafter positioning at least one integrated circuit device below said wiring bond pad to thereby conserve integrated circuit space and improve wiring bond pad efficiency as a result of configuring said wiring bond pad as a single metal layer, wherein said single metal layer comprises a single metal layer isolated from other layers and metals of said wiring bond pad;

thereafter locating said wiring bond pad above a plurality of intermetal dielectric layers, wherein said plurality of intermetal dielectric layers comprises at least IMD-1 to IMD-7 layers; and

thereafter forming a layer of aluminum film above said wiring bond pad, such that said layer of aluminum film comprises a thickness of approximately 15KÅ, wherein said layer of aluminum film above said wiring bond pad comprises a buffer and bonding layer, thereby preventing a wiring bond stress-induced facture in said wiring bond pad.

40. (Previously presented) The method of claim 39 wherein said layer of aluminum film above said wiring bond pad comprises a bonding layer.